OIPE JC73
MAR 0 3 2003
PATENT & TRADEMARK OFFICE

RS
#2
8-14-04

PATENT APPLICATION

Docket No.: 3902 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	DEAS, Alexander, Roger; ABROSIMOV, Igor Anatolievich
Serial No.:	10/038,868
Filed:	01/08/2002
Art unit:	2123
Confirmation No.	8180
Examiner:	Not assigned yet
For:	RECEIVER WITH AUTOMATIC SKEW COMPENSATION

Assistant Commissioner for Patents
Washington, D.C. 20231

February 25, 2003

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Sir:

In accordance with the duty of disclosure under 37 C.F.R. §§ 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached Form PTO-1449 and/or listed herein and which the Examiner may deem material to the patentability of the claims of the above-identified application.

The following prior art (1-10) was cited by Examiner in the Office Action issued by the GB Patent and Trade Mark Office in relation to co-pending GB application 0131100:

1. EP O 797 326 (Texas), filed 18.02.97, publ.24.09.97;
2. EP O 575 000 (Philips), filed 14.06.93, publ.22.12.93;
3. EP 0 193 332 (NEC Corp.), filed 18.02.86, publ.03.09.86;
4. US6,127,864 (Mission Research Corp.), filed 19.08.98, issued 03.10.2000;
5. US 5,018,142 (Digital Equipment Corp.), filed 26.01.90, issued 21.05.91;
6. US 4,965,884 (Northern Telecom Ltd.), filed 22.11.89, issued 23.10.90;
7. US 4,891,812 (Motorola), filed 09.12.85, issued 02.01.90;
8. US 4,771,421 (Telefonaktiebolaget LM Ericsson), filed 09.07.86, issd.13.09.88;
9. US 4,432,094 (Siemens Aktiengesellschaft), filed 27.08.81, issued 14.02.84;
10. US 4,241,311 (Telex Computer Products), filed 01.02.79, issued 23.12.80.

Additionally, the Applicants refer the Examiner to the following publications (11-16):

11. US 2002/0085656 (Sang-Hyun Lee), filed 29.08.2001, publ.04.07.2002;
12. US 6,374,361 (Silicon Image, Inc.), issued 16 April 2002;
13. US 6,229,859 (Silicon Image, inc.), issued 8 May, 2001;
14. US 5,905,769 (Silicon Image, inc.), issued 18 May, 1999;
15. A 5-Gb/s 0.25–μm CMOS Jitter-Tolerant Variable–Interval Oversampling Clock /Data Recovery Circuit by Sang–Hyun Lee, et al., IEEE Journal of Solid - State Circuits, Vol.37, No. 12, December 2002.
16. US 2001/0031028 (Cicero Silveira Vaucher), filed 05.03.2001, publ.18.10.2001;

One copy of the each of the listed documents is submitted herewith.

The present Information Disclosure Statement is being filed: (1) Before the mailing date of the first Office Action on the merits; or (2) Before the mailing date of the first Office Action after filing a request for continued examination (RCE) under §1.114, and therefore, no Statement under 37 C.F.R. §1.97 (e) of fee under 37 C.F.R. §1.17 (p) is required.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the preset application.

Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

REMARKS

The Applicant would like to make the following comments.

1. With respect to documents 1-10 cited by GB PTO, the following shall be noted.

Generating several signal samples over time (over-sampling) and combining the samples in a majority decision logic to determine the most likely outcome is well-known and used, for example, in US 4,771,421, US 4,241,311, US 4,965,884, US 5,018,142 and EP 0797,326, EP 0575,000 cited by the GB PTO.

Thus, US 4,771,421 describes a system comprising sampling means having inputs connected to the outputs of shift registers for giving an indication of a particular binary value when more than a predetermined number of outputs of shift registers show an one-bit value. However, no BER distribution is taken into consideration, therefore, it would be impossible "to produce a combined signal having the Bit Error Rate Distribution narrower than the distribution of a single signal copy".

US 4,241,311 describes a system comprising means for sampling a signal at the times of clock signal, and apply the stream of sampled signal bits to a digital shift register and on to majority gates. No selection of the best copy is disclosed. No polyphase clocking.

In US 4,965,884, a system is described comprising sampling means and means for choosing a data sample representing a majority of the data samples. No BER estimation is made.

US 5,018,142 describes a system comprising a sampler for sampling incoming signals and employing majority circuits to change the value of any samples that are not part of a plurality of sequential samples of the same value. No BER distribution is estimated.

US 6,127,864 describes a system that samples data at three different times and also outputs a majority signal at the forth time. No BER estimation is made.

EP 0 575 000 describes a system having a majority logic arrangement for estimating data from a noisy data signal, which monitors the data samples entering and leaving a shift register and a transition between "1" state and "0" state.

EP 0 797 326 describes a method comprising the steps of receiving a signal, sampling the signal at a predetermined sampling rate, generating a second and third samples by shifting the first sample, whereupon the samples are compared to one another and a majority sample value is obtained which represents the corrected signal value.

Though the above described approaches involves over-sampling of several signals, no BER distribution function of a signal is taken into consideration in none of the above described technique. At the same time, it shall be understood that, due to BER distribution has a probabilistic nature, even if some BER values are estimated in this or that way in some of the prior art references, the discrete character of the estimation would not allow to make an exact judgement of the extremis position in the curve and hence, the exact determination of the position of a sample having minimum BER value. The inventive approach of the present application involves obtaining and using information relating to BER function distribution that enables to determine properly the sampling position even in case when discreet data do not show it.

According to another known approach, the Bit Error Rate is measured for a signal decided as having the least BER by majority and compared with each of the repeatedly received patterns.

Again, it shall be well understood that in high-speed communications, it is absolutely not evident that the majority signal would have a better quality than separate signals combined by majority. Due to the higher data rate required in high speed communications, the channel bandwidth is occupied mostly by data that makes it impossible to rely upon majority decisions without the precise estimation of the sampling position with respect to eye window.

In EP 0193,332 an apparatus for processing a digital signal is described wherein a particular signal pattern with the least error rate is determined by majority logic. The signal pattern is transmitted repeatedly, and processed in a receiver by measuring the Bit Error Rate in a transmission path with the majority signal pattern equivalently used as a reference. Thus, the signal copies are produced by a transmitter, not by a sampling system, therefore the copies may differ in frequency, noise characteristics, etc.

In US 4,891,812, a method is described comprising the steps of generating a majority signal from at least three signals, determining the BER for each signal by bit-by-bit comparison with the majority signal, and selecting either one of the signals or the majority signal. Again, the signals are coming via separate channels and produced by a transmitter, not by a sampling system, thus, the system does not improve the quality of the signal received, but chooses a signal of better quality among several signals. The BER is estimated between different channels with respect to majority signal and does not reflect the BER distribution within a separate channel as a function of phase of the sampling clock.

According to US 4,432,094, a method comprises sampling the signal at different times and deciding by majority the signal with the lowest information error rate. However, the samples are taken at multiple of the information clock frequency that does not allow to use this technique in the high speed interfaces because it is impossible to generate multiple frequencies when the information clock frequency is already near the maximum achievable in this particular technology.

Furthermore, according to the above discussed and other patents, such as US 6,111,911 mentioned in the specification, a high degree of chip code synchronization is used to clock the data bit position. Transmitters transmit a data bit in synchronization with the chip code pattern, therefore allowing chip position to be used as a cue to the associated data bit position. Since the optimal position in which to sample a data bit is known, that portion of the Bit Error Rate loss is eliminated. Empirical results from this technique have shown practical improvements in the error rate versus carrier-to-noise ratio in the minimal detectable signal case. This technique is applicable to any direct sequence spread spectrum system in which a high degree of synchronization is inherently achieved, provided that the data is transmitted in synchronization with the chip code clock.

However, very often, in particular, in high speed communications, such a synchronisation is not effective, while the Bit Error rate is defined by the current application system requirements. The more strict are these requirements, the lower is the data rate providing the desired Bit Error level.

A special case of this applies to where a communication channel uses clock recovery, that is, the clock is recovered from the signal, as in US 4,891,812 discussed above, and this is used to latch the received data. This approach does, to a limited degree, reduce the effect of low frequency noise, such as environmental changes. However the problem with this approach is that the entire error in the clock recovery system or the phase detectors is added to the noise in the channel and for very high frequency applications, this inaccuracy becomes a significant problem.

Therefore, still another important feature of the present invention is the use of a polyphase clock to spread the sample copies in time. As mentioned in page 14 of the specification of the present application, the polyphase clock can be generated using a ring oscillator with each clock phase being taken from each inverter stage of the oscillator. Some extra phase splitters can be used for finer granularity. With the polyphase clock, the sampling points of each of register are spread in time by virtue that they are clocked at slightly different instances in time.

2. The Applicants further have become aware of the prior art listed as 11-16 and would like to note the following.

A system disclosed in US 5,905,769 (ref. 14) comprises an oversampler, a digital phase-locked loop (DPLL) and a bite synchroniser. The oversampler samples a digital signal under control of a multiphase clock and produces a sequence of oversampled data. The DPLL receives the sampled data and selects samples based on skew characteristics of the sample. A phase error is detected by oversampling a data signal to generate a string of binary samples, combining samples including a previous sample, the bit string and a next sample and selecting a subset of the composite string in response to a phase selection signal. However, no BER is estimated and no BER distribution is determined and taken into account that prevents from producing a signal having minimum BER.

A receiver described in US 6,229,859 (ref.13) comprises an oversampler, a digital phase-locked loop (DPLL) and a frame aligner. The oversampler samples a data stream and produces an oversampled data stream. The DPLL receives the sampled data, extracts clock information and selects data using the clock information. Further, a signal is generated indicating positions of data transitions in the oversampled data stream, so as to determine a phase at which to select data. No BER estimation is made and no BER distribution is determined.

An apparatus for correcting skew is disclosed in US 6,374,361 (ref.12). The apparatus comprises an oversampler, a digital phase-locked loop (DPLL) and a bite synchroniser. A skew is removed by generating multiple clock signals and sampling the data at multiple intervals, using the samples to eliminate skew. Alternatively, a sample array samples transitions between two adjacent serial bits of data and also a

center position of each serial bit of data. No BER estimation is made and no BER distribution is determined.

A data recovery system described in US 2002/0085656 (ref. 11) includes a data sampler, a compare logic, a phase controller and a phase shifter. Data sampling phases are split so as, first, to track the data eye to select an optimal sample position using a phase shifter and, then, to sample the signal. Contrary to this, according to the present invention, the signal is sampled first, and then a signal with minimal BER is selected. Further, according to approach described in US 2002/0085656, the bit error rate (BER) is measured by comparing data samples to obtain a so-called pseudo-bit error rate based on which the data sample is selected. Though discreet pseudo-BER values are estimated for signal samples, a small number of clocks (3) do not allow to estimate the complete BER distribution (it is neither proposed, nor surmised), thereby preventing from making a valid selection of a sample having a factual minimal BER.

A data clocked recovery circuit described in US 2001/0031028 includes a phase detector logic, a clock oscillator which comprises parallel data samplers (2 clock phases per bit), and a BER detector logic. The BER detector logic detects the presence or absence of BER by comparing a current data sample with a reference formed by 2 equal signal samples. No BER value is estimated and no BER distribution is determined, so that no sample having a factual minimal BER can be produced.

Thus, the approaches described above in references 11-16 involve over-sampling of several signals, while some involve also the use of multiphase clocks. However, no BER distribution function of a signal is taken into consideration in none of the above described technique. At the same time, as has been discussed above, even if some BER values are estimated, or the presence or absence of BER is detected, this would not allow to determine the actual extremis position in the BER distribution curve preventing from producing a sample having minimum BER value. The inventive approach of the present application involves obtaining and using information relating to BER function distribution that enables to determine properly the sampling position even in case when discreet data do not show it.

By presenting the above discussion of the prior art, the Applicants by no means wish to influence the opinion of the Examiner, but have a bona fide intention to make a detailed explanation of the invention and its specific features in comparison to the available prior art.

Respectfully submitted,

February 25, 2003

Alex Deas
alex@acuid.com

Igor Abrosimov
igor@acuid.com

Tel. +7 (812) 325 6454
+7 (812) 325 9842
Fax: +7 (812) 325 5208
Contact person: Maria Nilova
e-mail: m_nilova@patentica.com

OIPE
MAR 0 3 2003
PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Rev. 2-32) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO. 10/038,868	DOCKET NO. 3902 US
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	APPLICANTS **DEAS, Alexander, Roger; ABROSIMOV, Igor Anatolievich**	
	FILING DATE **January 8, 2002**	

RECEIVED
MAR 0 4 2003
Technology Center 2100

U.S.PATENT DOCUMENTS

Examiner Initial	Cite No.	Document Number	Date MM-DD-YYYY	Name of Patentee or Applicant	Class	Subclass	Filing date if appropriate
	1	6,127,864	10-03-2000	Mission Research Corporation	327	144	
	2	5,018,142	05-21-1991	Digital Equipment Corporation	370	112	
	3	4,965,884	10-23-1990	Northern Telecom Limited	375	106	
	4	4,891,812	01-02-1990	Motorola, Inc.	371	5.5	
	5	4,771,421	09-13-1988	Telefonaktiebolaget LM Ericsson	370	85	
	6	4,432,094	02-14-1984	Siemens Aktiengesellschaft	375	94	
	7	4,241,311	12-23-1980	Telex Computer Products, N.C.	328	167	
	8	6,374,361	04-16-2002	Silicon Image, Inc.	713	503	
	9	6,229,859	05-08-2001	Silicon Image, Inc.	375	354	
	10	5,905,769	05-18-1991	Silicon Image, Inc.	375	376	
	11	2002/0085656 A1	07-04-2002	Sang-Hyun Lee et al.	375	355	
	12	2001/0031028 A1	10-18-2001	Cicero Silveira Vaucher	375	355	

FOREIGN PATENT DOCUMENTS

Examiner	Cite No.	Document Number	Date MM-DD-YYYY	Country	Class	Subclass	Translation YES/NO
	1	EP 0797326 A2	09-24-1997	DE, FR, GB, IT, NL	H04L 1	00	
	2	EP 0575000 A1	12-22-1993	CH, DE, FR, GB, IT, LI	H04L 25	38	
	3	EP 0193332 A2	09-03-1986	DE, FR, GB, NL	H04L 1	08	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

	1		A 5-Gb/s 0.25 μm CMOS Jitter-Tolerant Variable-Interval Oversampling Cock/Data Recovery Circuit by Sang-Hyun Lee, et al., IEEE Journal of Solid – State Circuits, Vol/ 37, No. 12, December 2002

EXAMINER DATE CONSIDERED